A 2.5 GHz Low Noise High Linearity LNA/Mixer IC in SiGe BiCMOS technology

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Abstract **A monolithic low noise high linearity LNA/Mixer circuit for 2.5 GHz applications has been fabricated in IBM 47 GHz SiGe production process. The measured performance is 8 dBm input IP3, 1.6 dB NF and 12 dB Gain for a low noise amplifier (LNA), and 2.5 dBm input IP3, 7.5 dB NF and 14 dB gain for a downconversion mixer with a total current consumption of 26 mA for a 2.75V supply. LNA matching, mixer RF and LO matching and two baluns are all integrated on chip, requiring no critical RF tuning components.**

I. Introduction

LNA and downconversion mixers are two main building blocks in receiver front end of cell phones. The phones work in a hostile environment of interferers to receive the weak wanted signals. The interferers are filtered after the first downconversion at IF by SAW filters. The SAW filters for wideband modulation schemes like CDMA/WCDMA have higher insertion loss (>10dB) than narrowband modulation ones like DECT/TDMA (~4dB). In order to achieve receiver sensitivity and dynamic range, low noise, sufficient gain and high linearity is required for components preceding SAW filter. It becomes a circuit design and technology challenge to achieve the performance with minimum power dissipation from the battery.

J. Long and M. Copeland [1] first reported a 1.9 GHz LNA and doubly balanced mixer using monolithic inductors and balun transformers on Silicon to lower the operating voltage and current. Their LNA had 2.8 dB NF, 9.8 dB Gain and –3 dBm input IP3 with 2.0 mA and their Mixer achieved NF 11 dB, 6 dB Gain and IP3 2.3 dBm with 2.5 mA. The design was done on 0.8 μm Si BiCMOS process with NPN *ft* of 11 GHz. By replacing the transconductor of the Gilbert cell with a center tapped transformer and feeding the RF to the switching quad via a transformer balun, the authors achieved more headroom for output voltage swing. The mixer RF port is single-ended 50 Ω and matches directly with an external image reject filter. This mixer works very well for supply voltages as low as 1.9V. The transformer coupled mixer (TCM) design also appears in other publications [2,3,4].

To overcome the high SAW filter loss in wideband systems, higher than 10 dB power gain is required from the mixer. In order to obtain high power gain while retaining input IP3 (IIP3), IF load can be increased up to a couple of kilo-ohms at 200 MHz IF until the mixer becomes supply voltage limited. When the current is increased to realize higher gain, the differential RF impedance (proportional to 1/gm) looking into the coupled emitter pairs of the Gilbert quad decreases. This makes the on-chip RF impedance transformation to 50Ω source lossy and increases Noise Figure. Modifying the TCM mixer in [1-4] by applying RF to the base of the core and LO to the emitter, low noise, high gain and output swing can be achieved simultaneously. The differential RF impedance can be designed to be 50 Ω by NPN device sizing (Cπ is area dependent and can be adjusted to give Zrf proportional to gmLe/Cπ) thus making the transformation 1:1 and low loss.

In this paper, a 2.5 GHz fully integrated low noise high linearity LNA and modified transformer coupled Mixer circuit with a LO amplifier is reported. Internally matched LNA achieves 1.6 dB NF, 12 dB Gain and 8 dBm IIP3 for a 7.5 mA current. The mixer achieves 14 dB Gain, 7.5 dB SSB NF (including balun losses) and 2.5 dBm IIP3 with 15 mA current for 2.75 V supply. Both the RF and LO baluns are integrated to enable the chip to be directly connected to a 50 Ω single-ended image reject filter and LO source. The design was implemented in 0.5 μm SiGe BiCMOS process with NPN *ft* of 47 GHz. To the best of our knowledge, this LNA/Mixer IC has one of the lowest noise figure and highest linearity reported for internally matched LNA /mixers at 2.5 GHz.

II. System Architecture

The chip architecture is shown in Fig. 1. The 3.24 mm2 die is mounted in a 16 pin plastic package (TSSOP16) with exposed paddle. The LNA is optimized in frequency range of 2.4-2.5 GHz. The signal goes off-chip from the

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LNA to an external image-rejection filter and is then fed back to the mixer. The 2.5 GHz single-ended RF input is converted to be differential to feed in the double balanced mixer by use of an on-chip balun. The mixer is driven by an on-chip local oscillator (LO) buffer amplifier. The LO frequency is at 2.3 GHz. The intermediate frequency (IF) is centered at 200 MHz. The differential IF output is then fed to differential IF SAW filter. The circuit has sleep mode with Enable pin as the power control.

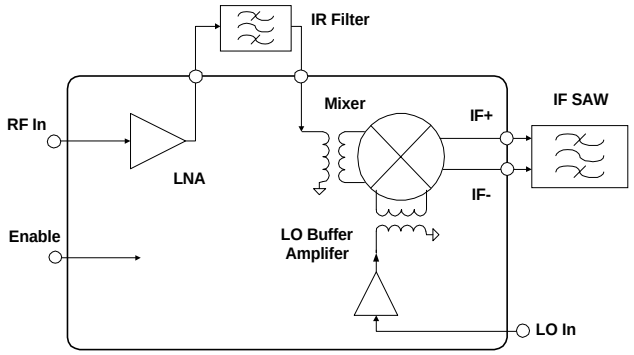

Figure 1. System Configuration

II. Circuit Design Considerations

The circuit consists of three major blocks, LNA, Mixer and LO buffer amplifier as well as all the matching blocks. The circuit also shared a common bandgap circuit, which provides constant current source for all blocks.

In order to achieve the low noise figure and high linearity, a single stage common emitter amplifier with emitter inductive degeneration is chosen shown in Figure. 2. Input impedance matching is achieved via bond wire,

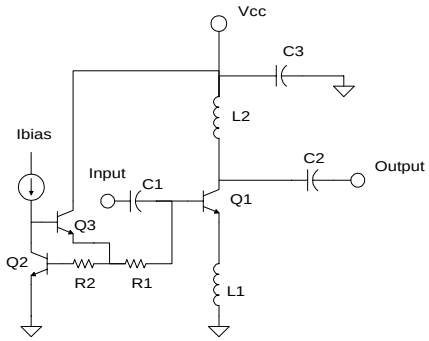

Figure 2. LNA simplified schematic

careful choice of dual strips NPN device Q1 (0.5µm x 5µm x 6) and degeneration inductor L1 (1nH). The device size and inductor L1 also affects the output power compression point. The current in transistor Q1 is 5.6 mA. Output impedance matching is achieved via on-chip pull-up inductor L2 and capacitor C2 as well as bond wire.

The mixer circuit illustrated in Figure 3 utilizes a simple Gilbert core as in publications [1-3] with the following modification: RF input is coupled into the base through a 1:1 on-chip balun while LO is coupled to the emitter. The doubly balanced Quad transistors (Q1- Q4) have a size of 0.5µm x 5µm x 8 each with 4 on-chip degeneration inductors (L1-L4 of 1.3 nH each). The NPN and degeneration inductor sizing has direct impact to the RF differential impedance looking into the base, given by Zrf proportional to gmLe/Cπ, where Cπ is related to NPN size. Each NPN is biased at 3.7 mA current. The emitter inductive degeneration improves significantly the linearity for RF when it is fed from the base. The on-chip balun loss at the input directly adds to the noise figure, so it was optimized for minimum loss.

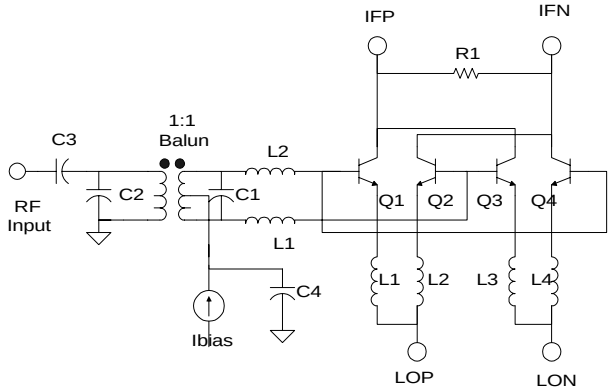

Figure 3. Mixer simplified schematic

LO buffer amplifier is a single stage common emitter amplifier with inductive degeneration (L1=3.75 nH). It has single ended input. A 4:1 on-chip balun is implemented at the output to match the impedance and drive the mixer differentially, shown in Figure 4. Input matching is realized by an on-chip inductor L3 and a shunt capacitor C4, together with the bond wire. The output matching is achieved through a pull-up inductor L2 and capacitor C2 as well as carefully tuning 4:1 baluns with two capacitors (C5 and C6). The typical LO input power level is 0 dBm. The input compression point of the buffer amplifier is designed to be slightly lower than the lowest LO power level allowed (-3 dBm).

Two on-chip baluns are designed and implemented in this circuit. The 1:1 balun is made of two tightly coupled inductors with a Q of about 15. The 4:1 balun is made of two pair of coupled inductors with primary side wired in

series and secondary side in parallel. With proper capacitor tuning, the losses are 1.5 dB, 2 dB for 1:1 balun, 4:1 balun respectively. In addition to improvement in power efficiency, on-chip baluns provide good isolation and noise rejection but with the price of more chip area.

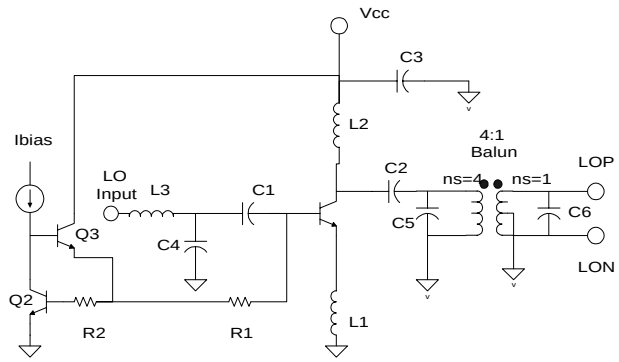

Figure 4. LO Buffer Amplifier simplified schematic

The biasing circuit consists of a bandgap circuit and an operational amplifier as a buffer to provide the constant current source. This constant current sets the different currents needed for all RF blocks (LNA, Mixer as well as LO buffer amplifier) by having different PFET mirror ratios. A constant current biasing is found to be essential to maintain the input compression point at low temperature, while sacrificing a little gain degradation at high temperature.

III. Measured Circuit Performance

Microphotograph of the front-end receiver circuit (LNA/Mixer) is shown in Figure 5. The IF port was converted and matched to 50 ohms from differential to single end by means of an external 4:1 balun and two matching components for test purpose. All other ports for LNA and Mixer are internally matched single-ended to 50 Ω. The packaged part was mounted on FR4 PCB evaluation board. Table I summarizes the measured performance for both LNA and Mixer, with the comparison to the simulated results.

The total current consumed is 26 mA with 7.5 mA in LNA, 15 mA in Mixer and 3.5 mA in LO buffer amplifier. The measured LNA gain is 12 dB, which is 1 dB less than that of simulated. The discrepancy of the gain is mainly due to the package and layout parasitic. Both input and output VSWR is about 2:1. The noise figure of LNA is measured at 1.6 dB, in good agreement with the simulation. The input P1dB and IIP3 are measured to be –4 dBm, 8 dBm respectively. IM2 of LNA is -50 dBm with -30dBm input levels, close to the simulated.

TABLE I
SUMMARY OF LNA AND MIXER MEASURED RESULTS

Parameter	Simulated	Measured
LNA		
Current	7 mA	7.5 mA
Gain	13 dB	12 dB
Noise Figure	1.55 dB	1.6 dB
Input IP3	6 dBm	8 dBm
Isolation	19 dB	19 dB
Mixer		
Current (W/ LO buffer)	17.5 mA	18.5 mA
Conversion Gain	14.5 dB	14.0 dB
SSB NF	7.0 dB	7.5 dB
Input IP3	3 dBm	2.5 dBm
LO_RF Isolation	50 dB	38 dB

Measured mixer conversion gain (14 dB) agrees quite well with the simulated. The Mixer has 1.5:1 input VSWR and LO buffer has 2:1 input VSWR. The gain remains flat for LO level from -3 dBm to 3 dBm. SSB NF is measured to be 7.5 dB including on-chip balun losses at RF input. The input P1dB and IIP3 are -7 dBm and 2.5 dBm respectively. IM2 is measured to –65 dBm with –30dBm input levels. The half IF spur is –62 dBc, indicating a well-balanced layout for mixer core.

Assuming that off-chip image reject filter has 3 dB insertion loss, the cascaded LNA/Mixer at the normal condition would achieve a performance of 23 dB Gain, 3.4 dB NF, IIP3 of –6.4 dBm for a power consumption of 72 mW.

IV. Conclusions

A 2.5GHz low noise high linearity LNA/Mixer IC has been designed and fabricated in BiCMOS SiGe technology. The measured performance is 8 dBm input IP3, 1.6 dB NF and 12 dB Gain for LNA, and 2.5 dBm IIP3, 7.5 dB NF and 14 dB gain for a downconversion mixer with LO buffer amplifier. The biasing bandgap circuit and constant current source is shared between LNA and Mixer. The matching circuits including all inductors and transformers are realized on-chip, requiring minimum amount of off chip matching components. The total

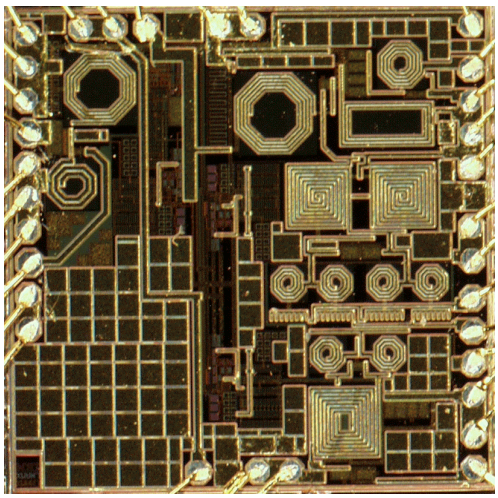

Figure 5. Microphotograph of the chip

current consumption is 26 mA for a 2.75V supply. A good agreement between measured and simulated results was achieved. The overall noise and linearity performance for LNA/Mixer is believed to be one of the best reported for wideband 2.5GHz application.

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